N- AND P-TYPE SiGe/Si SUPERLATTICE COOLERS

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ABSTRACT

SiGe is a good thermoelectric material for high temperature applications. In this paper the fabrication and characterization of single-element SiGe/Si superlattice coolers of both n- and p-type devices are described for room temperature applications. Superlattice structures were used to enhance the device performance by reducing the thermal conductivity between the hot and the cold junctions, and by providing selective removal of hot carriers through thermionic emission. The structure of the samples consisted of a 3 μm thick symmetrically strained $Si_{0.7}Ge_{0.3}$/Si superlattice grown on a buffer layer designed so that the in-plane lattice constant is approximately that of relaxed $Si_{0.9}Ge_{0.1}$. Cooling by 1.7 K for n -type device and by 1.9 K for p-type device at room temperature was measured, corresponding to cooling power densities of hundreds of watts per square centimeter. The results show that the packaged devices of both n and p coolers can work together in similar optimal conditions. This paves the road to fabricate n- and p-type superlattice coolers in an array format electrically in series and thermally in parallel, similar to conventional thermoelectric devices, and thus achieve large cooling capacities with relatively small currents.

KEY WORDS: SiGe, superlattice, cooler, silicon, thermionic, thermoelectric, integration

INTRODUCTION

With the rapid development of very-large-scale-integration (VLSI) technology, the number of components per integrated circuit (IC) chip is increasing considerably and the power density increases accordingly. Device performance and reliability degrade significantly when devices are overheated. Heat generation and thermal management are becoming one of the barriers to further increases in clock speed and decreases of feature size. Thermoelectric (TE) coolers based on Bi_2Te_3 are commonly used for electronic and optoelectronic device cooling, but they can not be directly integrated with the IC manufacturing process. Solid-state coolers integrated with VLSI devices are an attractive way to solve some of these problems.

SiGe is a good thermoelectric material for high temperature refrigeration and power generation applications [1]. In this paper we describe the fabrication and characterization of single-element SiGe/Si superlattice coolers that use thermionic and thermoelectric effects. Both n- and p-type devices have been fabricated. Superlattice structures can enhance the cooler performance by reducing the thermal conductivity between the hot and the cold junctions [2] and by selective emission of hot carriers above the barrier layers in the thermionic emission process [3]. Si and SiGe devices can integrate directly with these coolers to achieve better device performance.

MATERIAL STRUCTURE

N- and p-type SiGe/Si superlattice structures were grown in a Perkin-Elmer Si molecular beam epitaxy (MBE) growth chamber on five-inch diameter, (001)-oriented Si substrates doped to <0.020 Ω-cm with Sb for the n-type devices and to <0.006 Ω-cm with B for the p-type devices.

The sample structure is shown in Figure 1. The structure consists of a 3 μm thick $Si_{0.7}Ge_{0.3}$/Si superlattice grown symmetrically strained on a buffer layer designed so that the in-plane lattice constant approximated that of relaxed $Si_{0.9}Ge_{0.1}$. The doping levels are 2×10^{19} cm^{-3} and 5×10^{19} cm^{-3} for n- and p-type SiGe/Si superlattices, respectively.

0.5μm $Si_{0.9}Ge_{0.1}$ cap layer
3 μm 200 × (5 nm $Si_{0.7}Ge_{0.3}$ / 10 nm Si) superlattice
1.15 μm (n) or 2μm (p) $Si_{0.9}Ge_{0.1}$/$Si_{0.845}Ge_{0.150}C_{0.005}$ buffer layer
Si substrate

Fig. 1 Material structure for the SiGe/Si superlattice coolers (not to scale)

For the relaxed buffer layer, we grew a 10-layer structure, alternating between 150 nm $Si_{0.9}Ge_{0.1}$ and 50 nm $Si_{0.845}Ge_{0.150}C_{0.005}$, roughly following the method suggested by Osten et al. [4]. For the n-type sample, the layers were grown

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at 390 °C and annealing was performed at 750 °C for 10 minutes after the growth of each $Si_{0.9}Ge_{0.1}$ layer. In the p-type case, the growth temperature was simply alternated between 700 °C for the $Si_{0.9}Ge_{0.1}$ layer and 500 °C for the $Si_{0.845}Ge_{0.150}C_{0.005}$ layer. After the relaxed buffer sequence, another 150 nm thick $Si_{0.9}Ge_{0.1}$ layer was grown at 390 °C in the n-type case and in the p-type case, a 1 μm thick $Si_{0.9}Ge_{0.1}$ layer was grown at 700 °C. Growth of a 200 period, 5 nm $Si_{0.7}Ge_{0.3}$/ 10 nm Si superlattice then followed at 390 °C (n-type case) and 500 °C (p-type case). Finally, the samples were capped with a heavily doped $Si_{0.9}Ge_{0.1}$ layer sequence to provide for a low-resistance holmic contact.

DEVICE FABRICATION AND TEST RESULTS

Mesas 3.6 μm high were formed using reactive ion etching down to the SiGe buffer layer to form the devices. A scanning electron microscope (SEM) image of the processed devices is shown in Figure 2.

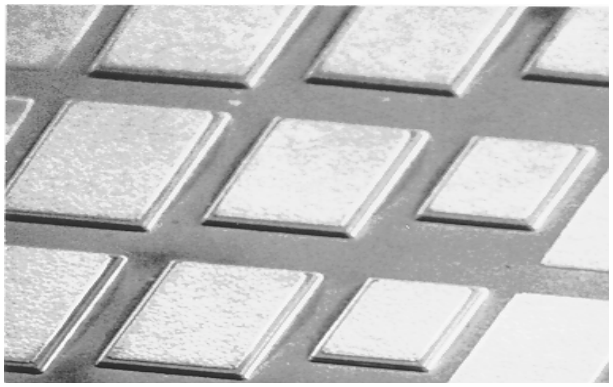

Fig. 2 A SEM image of the processed SiGe/Si superlattice cooler devices

Electrical contact resistance is an important factor for device performance. A 100 nm titanium metal layer was first deposited, which was intended to form a titanium silicide on the silicon surface and to act as a metal barrier to separate Si and Al. Subsequently 1μm thick aluminum layer was deposited. To facilitate wire bonding, an additional metal layer of titanium and gold was used. Annealing was accomplished at temperatures between 450 °C and 550 °C. TLM (transmission line method) measurements were carried out and the results are shown in Figure 3. The measured specific contact resistivity is about 4×10^{-7} Ω-cm^2 for both n- and p-type devices.

Devices were tested with a heat sink temperature from 25 °C up to 70 °C. Cooling temperatures were measured with micro thermocouples. Large devices (150×150 μm^2) were tested directly with probes, while smaller devices (100×100 μm^2 and 50×50 μm^2) were mounted in packages and wire bonded. Figure 4 displays the measured temperature on top of the 100×100 μm^2 devices as a function of current. The temperature is relative to the value at zero current. Despite the large thermal resistance of the Is substrate and package on the hot side of the cooler and Joule heating in the wires connected to the cold junction, a net cooling of 1.7 K and 1.9 K was observed on top of the n- and p-type devices respectively. This cooling over the small barrier thickness corresponds to cooling capacities on the order of 100 W/cm^2.

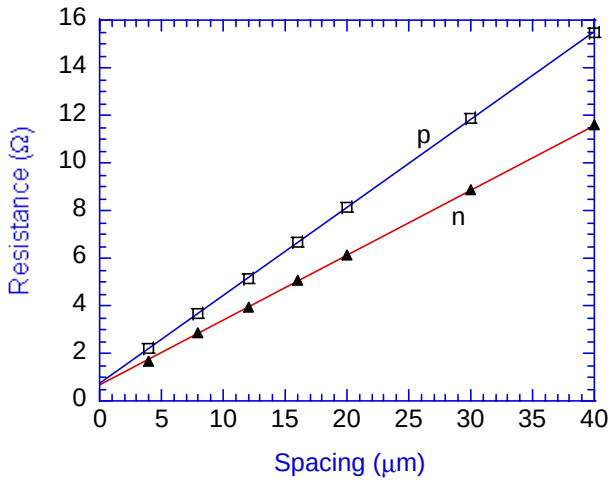

Fig. 3 n- and p-type SiGe ohmic contact TLM measurements with the doping for p-type SiGe at 2×10^{20} cm^{-3}, and n-type SiGe at 1×10^{20} cm^{-3}. The metal pad size is 50×100 μm^2. Space separation between measured pads is from 4 μm to 40 μm.

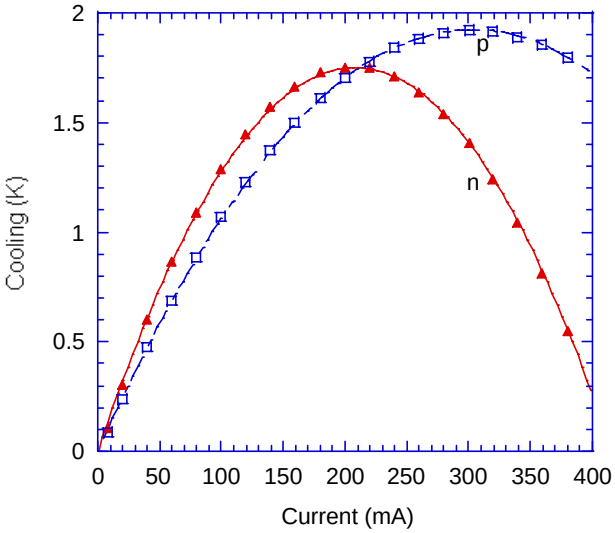

Fig. 4 Cooling measured on n- and p-type 100×100 μm^2 SiGe/Si coolers

Maximum cooling varies with device sizes and device substrate temperatures. Figure 5 shows cooling results of devices with different sizes. It was observed that the maximal cooling temperature increases as the device size decreases.

The measured cooling of 50×50 μm^2 p-type SiGe/Si devices at various substrate temperatures is shown in Figure 6. The device cools better at higher temperatures. The net cooling increased from 2.6 K at 25 °C to 4.2 K at 70 °C. The reason for the improved performance with the increase in temperature

is two fold. First, the thermal conductivity of the material decreases at higher temperatures [5, 6] and second, the thermionic emission cooling power increases due to the larger thermal spread of carriers near the Fermi energy.

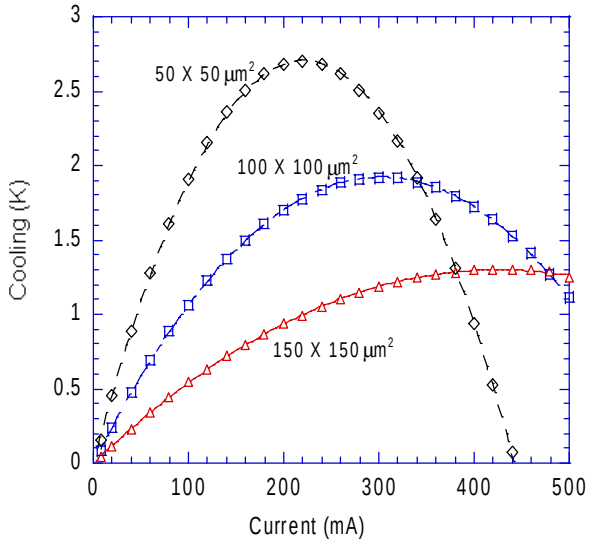

Fig. 5 Cooling measured on p-type SiGe/Si devices of different sizes

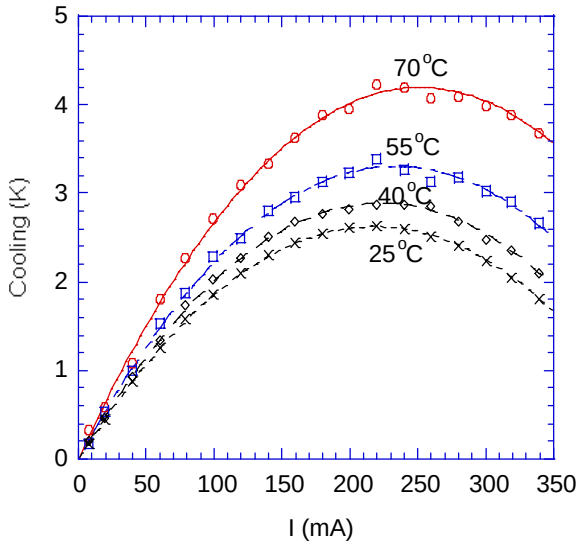

Fig. 6 Measured cooling on a 50×50 μm² p-type SiGe/Si cooler at various substrate (heat sink) temperatures

DISCUSSION AND ANALYSIS

Various factors affect the overall performance of the device. These include the electrical and thermal conductivity in different layers, especially for the SiGe/Si superlattice, selective emission of hot carriers above the superlattice barrier, thermoelectric effect at the junction between different materials, package thermal resistance, Joule heating in the wires connected to the cold junction, etc. Device size is an important factor in the device performance. Experimental results show that smaller devices attain better cooling. This cannot be explained with conventional ideal thermoelectric or thermionic cooler models. This is due to the 3D nature of current spreading in the substrate of the devices and the Joule heating from the bonding wires. For the same wire resistance, smaller devices require a smaller optimum current which is favorable for better cooling performance.

Further experimental analysis is continuing. A 3D finite-difference heat equation solver [7, 8] is being used to model the device performance. Based on the intrinsic properties of SiGe, integrated cooling by tens of degrees is possible.

CONCLUSIONS

SiGe/Si superlattice coolers were demonstrated and cooling of 1.7 K and 1.9 K were measured for n- and p-type 100×100 μm² devices. Cooling up to 4.2 K was obtained at 70 °C for p-type 50 x 50 μm² devices. The results show that the packaged devices of both n- and p-type coolers can work together in similar bias current conditions. This paves the road to fabricate n- and p-type superlattice coolers in an array format electrically in series and thermally in parallel, similar to conventional thermoelectric devices. Thus large cooling capacities with relatively small currents can be achieved and the problems of series resistance and heat load of contacting wires can be avoided.

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REFERENCES

[1] C. B. Vining: "A model for the high-temperature transport properties of heavily doped n-type silicon-germanium alloys," *Journal of Applied Physics*, Vol. 69, no.1, pp. 331-41, Jan. 1991.

[2] S.-M Lee, David G. Cahill and Rama Venkatasubramanian: "Thermal conductivity of Si-Ge superlattices," *Appl. Phys. Lett.*, Vol. 70, no. 22, pp. 2957-9, June 1997.

[3] Ali Shakouri and John E. Bowers: "Heterostructure Integrated Thermionic Coolers," *Appl. Phys, Lett.*, Vol. 71, no. 9, pp. 1234-6, Sept. 1997.

[4] H. J. Osten and E. Bugiel: "Relaxed $Si_{1-x}Ge_x/Si_{1-x-y}Ge_xC_y$ buffer structures with low threading dislocation density," *Appl. Phys. Lett.*, Vol. 70, no. 21, pp. 2813-5, May 1997.

[5] G. J. Glassbrenner and G. A. Slack: "Thermal Conductivity of Silicon and Germanium from 3°K to the Melting Point," *Phys. Rev.*, Vol. 134, no. 4A, pp. A1058 –69, May 1964.

[6] K.L. Wang and X. Zheng, in *Properties of Strained and Relaxed Silicon Germanium*, edited by Erich Kasper, London: INSPEC, pp. 70-8, c1995.

[7] Ali Shakouri, Chris LaBounty, Joachim Piprek, Patrick Abraham, and John E. Bowers: "Thermionic Emission Cooling in Single Barrier Heterostructure," *Appl. Phys. Lett.*, Vol. 74, No. 1, pp. 88-9 1999.

[8] Chris LaBounty, Ali Shakouri, Gerry Robinson, Patrick Abraham, John E. Bowers, "Design of Integrated Thin Film

Coolers," *Proceedings of the Eighteenth International Conference on Thermoelectrics*, Baltimore, MD, USA, Sept. 1999.